

One Week Joint Online Faculty Development Programme

Designing With FPGAs (Intel) Mar 12 – 17, 2022

Organized by
IIT Guwahati, IIT Roorkee, MNIT Jaipur, NIT Patna & PDPM IITDM Jabalpur



Course Contents

- Introduction to Intel FPGAs and Quartus tool flow
- Timing Analysis- Applying Timing Constraints- Clock Domain Crossing
- Introduction to High Level Synthesis, Intel HLS Compiler and System Integration
- Conversational AI, NLP and FPGA, Intel FPGAs for AI
- FPGA Acceleration and Acceleration Stack Overview
- Embedded System Design using Cyclone V and ARM
- Mini Project using Intel SoC FPGAs

Joint Principal Coordinator

Prof. V K Gupta
PDPM IITDM Jabalpur
Email: vkgupta@iiitdmj.ac.in
Ph: +91-761-2794413

Speakers from Intel

- Padmanaban K
- Bhaskar Venugopal
- Ipsita Das
- Raghavendra Bhat
- Nilesh Sable
- Praveen Kalappurakkal

Programme Features

- Instructor led online sessions and rigorous hands-on sessions.
- Rigorous Hand- on (practice)
- Special sessions on Simulation and characterization
- Specific industry-led sessions
- Opportunities to connect with expert for research orientation

Registration Details

Registration link –

<https://forms.gle/JWYaCyutTKiFUG8V9>

Registration fee

Indian Participants –

Academic (student/faculty): 500 INR

Industry Participants and Others : 1000 INR

Foreign Participants –

SAARC/African countries

Academic (student/faculty): - Rs. 500/-

Others - Rs. 1000/-

Rest of the countries

Fee - US\$ 60 or British £ 50

Last Date for Registration : Mar 4, 2022

Online payment details

Beneficiary Name : EICT Academy

Bank Name: INDIAN BANK

A/C No. : 50302042708

IFSC Code: IDIB000M694

Branch: Mehgawan, IIITDM Branch

Contact Us

Contact Us :

ritu.bhatnagar@iiitdmj.ac.in,

academy@iiitdmj.ac.in

Cell No: 8458849734

